Sessional Sessionals

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belgaum)

II Sem B.E. (Credit System) Mid Semester Examinations – I, January 2015

14EC112 – BASIC ELECTRONICS

Duration: 1 Hour

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

1. a) Sketch the typical V-I characteristics of Si and Ge diodes and mark the important points. 6

   b) Design a zener voltage regulator to meet the following specifications. 4
   DC input voltage, V_i=20V, dc output voltage V_o=10V, load current I_L=20mA, I_{Zmin}=10 mA, I_{zmax}=100mA.

2. a) What is a DC load line? Give the equation of DC load line of a diode in series with dc supply voltage and resistor R such that diode is forward biased. 6

   b) Discuss the types of junction breakdown that occur in reverse breakdown diodes. 4

Unit – II

3. a) Draw the circuit diagram of full wave rectifier using two diodes. Explain its principle of working with relevant waveforms. Also derive an expression for DC output voltage. 6

   b) The input to a half wave rectifier is given through a 10:1 transformer from a supply given by 230 sin 314t V. If R_f =50Ω and R_L=500Ω,determine
   (a) DC load voltage (b) RMS load voltage. 4

4. a) Draw the circuit of a full wave rectifier with capacitor filter. Explain its working with relevant waveforms. 6

   b) A full wave rectifier with capacitor filter is supplying a resistive load of 1000Ω.The value of filter capacitor is 200μF.If supply voltage to the rectifier is 200 V at 50Hz,Calculate RMS ripple voltage 4

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I/II Sem B.E. (Credit System) Mid Semester Examinations - II, March 2015

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14EC112 – BASIC ELECTRONICS

Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

Unit – I

a) Draw the circuit of **NPN** transistor in common base configuration. Sketch and explain input and output characteristics. Mark regions of operation on output characteristics. 6

b) ... in common emitter configuration operates with collector circuit d.c. supply of 24 volts. ... collector resistance and base bias resistance for base bias arrangement to have V_{CE} = 12 volts and I_C = 12 **mA** . Assume **β = 50.** 4

a) Draw the circuit of **NPN** transistor in common emitter configuration. Sketch output characteristics, mark regions of operation and explain. 6

b) With circuit diagram and waveforms explain operation of pulse firing circuit for half wave controlled rectifier using **SCR**. 4

Unit – II

a) With circuit diagram explain operation of Hartley Oscillator. If this Oscillator is to have output frequency of 100 KHz using two inductances of 100 μH and 10μH in the feedback network , what should be the value of capacitor in the feedback network ? Also calculate the gain required for the amplifier section of the circuit. 7

b) An amplifier having absolute voltage gain of **100** is cascaded with a second amplifier having power gain of **10 dB**. Determine the overall power gain in **dB**. 3

a) Sketch the frequency response of **R-C** coupled amplifier and mark relevant parameters and explain their significance. State reason for reduction in gain for low and high frequencies. 5

b) With block diagram explain the operation of series voltage negative feedback amplifier. Derive expression for closed loop gain. Mention features of this amplifier. 5

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NMAM INSTITUTE OF TECHNOLOGY, NITTE

(An Autonomous Institution affiliated to VTU, Belagavi)

I Sem B.E. (Credit System) Mid Semester Examinations - II, October 2015

15EC112 – BASIC ELECTRONICS

Duration: 1 Hour | Max. Marks: 20

*Note: Answer any **One** full question from **each Unit.***

		Marks	BT*
	Unit – I		
1. a)	Sketch and explain the output characteristics of the common base configuration of an NPN transistor with the help of circuit diagram. Mark the regions of operation on the characteristics.	6	L*3
b)	Calculate the values of R_C and R_B in a base bias circuit to have V_{CE}=6V and I_C = 6mA. The supply voltage is 12V and the transistor has β=100. Draw the circuit diagram and mark all the component values.	4	L4
2. a)	Sketch and explain the forward V-I characteristics of an SCR for different gate currents with the help of circuit diagram.	6	L3
b)	The base bias circuit arranged for maximum symmetrical output swing is to have collector resistor, R_C =2KΩ and quiescent value of V_{CE}=10V, β =50. Calculate i) Value of I_C at Q-point. ii) Value of R_B.	4	L4
	Unit – II		
3. a)	Draw the circuit of a non-inverting op-amp amplifier and derive its closed loop voltage gain.	6	L3
b)	For an inverting amplifier R_1=20KΩ and R_F=1MΩ. Calculate the closed loop voltage gain and required input voltage to get an output voltage of 2V.	4	L4
4. a)	With the help of a neat circuit diagram, derive the expression for the output voltage of integrator circuit using op-amp.	6	L3
b)	Design an adder circuit using op-amp to obtain the output voltage given by $V_0 = -(0.5V_1 + 0.8V_2 + 2V_3)$ where V_1, V_2 and V_3 are the input voltages and given R_F=10KΩ. Draw the circuit indicating all resistor values.	4	L4

* Bloom's Taxonomy, L* Level

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